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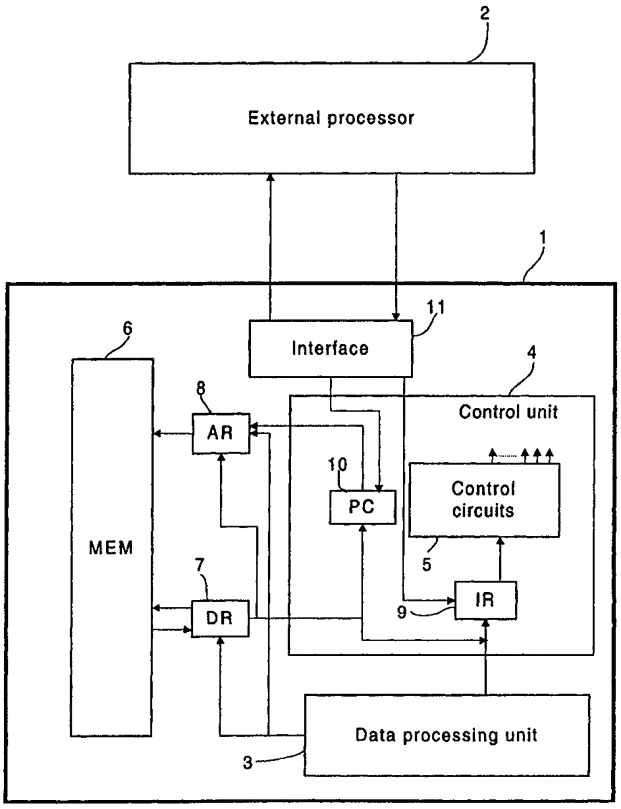
(54) Title: PROCESSOR AND METHOD OF EXECUTING INSTRUCTIONS FROM SEVERAL INSTRUCTION SOURCES

(57) Abstract

An internal processor (1) for the execution of instructions from several instruction sources (2; 6), wherein an interface (11) is connectable to at least an external instruction source (2), enabling execution interleaving of instructions from the instruction sources (2; 6), which is controlled by the external instruction source.



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TITLE: PROCESSOR AND METHOD OF EXECUTING INSTRUCTIONS FROM SEVERAL INSTRUCTION SOURCES

Field of the Invention

The present invention relates generally to a processor and a method of executing instructions from several instruction sources, and more particularly to an internal processor, wherein the execution of the internal processor is controlled by an external processor.

Description of the Prior Art

A conventional processor or CPU regularly comprises at least a processing unit and a control unit including various processing and control circuits as well as a set of registers intended for temporary storage of instructions, memory addresses, and data. The control circuits in the control unit are responsible for the machine or instruction cycle comprising the steps of fetching instructions, decoding opcodes, routing information to the intended entity, and providing proper control signals for all CPU actions. Program instructions and data are fetched from a primary memory.

However, in some cases it is desired to control a processor integrated on a general or special purpose chip. For example during the test phase or even during real operation of the chip it is desired to have the complete control of the execution and to read information of the internal state of the processor.

US-A-5 410 544 discloses an apparatus for testing a unit comprising an internal processor coupled to a register by an internal bus. In one embodiment the apparatus provides external control to a flash memory unit that has an internal processor. The internal processor is programmed so that it can execute an algorithm which performs an operation on the unit when it is executed. An internal bus

is used by the internal processor to access a state datum when the internal processor is executing the algorithm. The apparatus comprises an external processor disposed external to the unit and an interface and switch disposed on the unit. The interface is coupled to the internal and externally processors and is for receiving a plurality of commands from the external processor. Examples of commands that may be sent from the external processor to the interface unit is read status or read the memory. Included in the commands is an ability to order the internal processor to execute an algorithm that has been stored within the internal processor. By issuing another command, a "trap door" command, the external processor can take control of some registers and thereby simulate the execution of algorithms by the internal processor.

Summary of the Invention

According to the present invention an improved internal processor arranged on a chip is provided which permits control from an external processor in a transparent and efficient way.

This object is obtained by an internal processor, enabling execution of instructions from several instruction sources according to the invention. An interface arranged in the processor is connectable to at least an external instruction source, enabling execution interleaving of instructions from the several instruction sources, which execution is controlled by the external instruction source.

An advantage of the present invention is that the external processor can control the operation of the internal processor in an efficient way, and has the access to the internal state of the internal processor in the same way as the internal processor itself.

Brief Description of the Drawings

In order to explain the invention in more detail and the advantages and features of the invention references in the following detailed description of the preferred embodiment are made to the accompanying drawings, in which

FIG 1 is a block diagram of an internal processor according to the invention connected to an external processor; and

FIG 2 is a flow chart of the instruction cycle in the internal processor of FIG 1.

Detailed Description of the Invention

Referring to FIG 1, there is illustrated a processor or a CPU 1 capable of interpreting and executing programs. In some cases such a processor is integrated on a general purpose or special purpose chip. Therefore, the processor according to the invention is referred to as an internal processor. The internal processor according to the invention is designed to be controlled by another processor referred to as an external processor 2.

Similar to a general purpose processor one embodiment of the invention comprises a data processing unit 3 and a program control unit 4. The processing unit 3 further comprises different kinds of processing circuits not shown on the drawings and the control unit 4 comprises various control circuits 5. High speed registers are also included in the processor 1 for temporary storage of instructions, memory addresses, and data. The control unit 4 fetches instructions, decodes operation codes, generates control signals for the other components of the processor, and routs data and information through the different parts of the processor: registers, memory etc. In order to synchronize the different components a clock circuit, not shown in the drawings, is used to generate timing signals.

Programs and data are stored in a main memory and on chip main memory 6 in the embodiment. A transfer of data takes place between the memory 6 and a data register 7, and the memory address used is stored in an address register 8. An operation code of an instruction to be decoded and executed is stored in an instruction register 9. The address of the next instruction to be executed is stored in still another register referred to as a program counter 10.

During the instruction cycle of the processor a sequence of actions or operations takes place, which is illustrated by the flow chart in FIG 2.

According to the present invention, the next instruction to be executed (operation code and operand) is fetched from the interface 11 if an instruction is provided by the external processor 2, and loaded to the instruction register 9 in the control unit 4. The external processor may provide the internal processor 1 with a sequence of instructions, i.e an instruction stream. However, if no instructions are provided by the external processor 2 the next instruction is fetched from the main memory 6, RAM or cache. The instruction is decoded and interpreted by the control circuits 5 and executed by the data processing unit. The results are placed in a suitable register in the data processing unit 3 or in the main memory 6.

Thus, the two different instruction streams are provided by means of the two instruction sources: the main memory 6 and the external processor 2 via the interface 11. These two instruction streams are almost completely independent. The program counter 10 is the only direct interaction available between the two instruction streams.

While instructions are provided by the external processor they are fetched by the internal processor via the interface 11 and then executed. When no further instructions are provided by the external processor 2, it provides the program counter of the internal processor 1

with an address of the next instruction and the normal operation of the internal processor 1 proceeds. The program counter 10 is automatically incremented after the next instruction has been fetched. Hence, the external processor 2 can control the operation of the internal processor in an efficient way, but not reversely.

In order to operate in a proper way the external processor may in some cases need feedback information from the interface 11.

Although the invention has been described by way of a specific embodiment thereof it should be apparent that the present invention provides a processor that fully satisfies the aims and advantages set forth above, and alternatives, modifications and variations are apparent to those skilled in the art.

As mentioned above the processor can be a part of a general purpose or special purpose chip in other embodiments of the invention. Thus, the processor in some cases has a completely different design and comprises for example additional registers, such as special purpose registers to facilitate branch control, facilities providing simultaneous processing of more than one instruction, and different kinds of data processing capabilities etc. However, the processor still has an interface enabling at least two different sources from which the processor fetches its instructions, one of which sources controls the execution of the internal processor.

CLAIMS

1. An internal processor (1) for the execution of instructions from several instruction sources (2;6), c h a r a c t e r i z e d by interface means (11) connectable to at least an external instruction source (2), enabling execution interleaving of instructions from said instruction sources (2;6), controlled by said external instruction source.

2. An internal processor according to claim 1, c h a r a c t e r i z e d in that said interface (11) is connected to a program register (10) of said internal processor (1) for the execution sequence control of said internal processor (1) by said external instruction source (2).

3. An internal processor (1) according to claim 1 or 2, c h a r a c t e r i z e d in that said interface (11) is connected to an instruction register (9) of said internal processor (1) for the execution sequence control of said internal processor (1) by said external instruction source (2).

4. An internal processor (1) according to any of the preceding claims, c h a r a c t e r i z e d by a primary storage means (6) from which the processor fetches instructions.

5. An internal processor (1) according to any of the preceding claims, c h a r a c t e r i z e d by an external processor connected to the interface (11) and providing instructions to the internal processor (1).

6: A method of executing instructions from several instruction sources (2;6) in an internal processor (1), c h a r a c t e r i z e d by the steps of:

for each instruction provided by an external instruction source (2), decoding and executing said instruction; otherwise

fetching an instruction from another instruction source (6), decoding, and executing said instruction.

7. A method according to claim 6, c h a r a c t e r i z e d by the step of:

fetching an instruction from a location in said another instruction source (6) determined by the external instruction source (2).

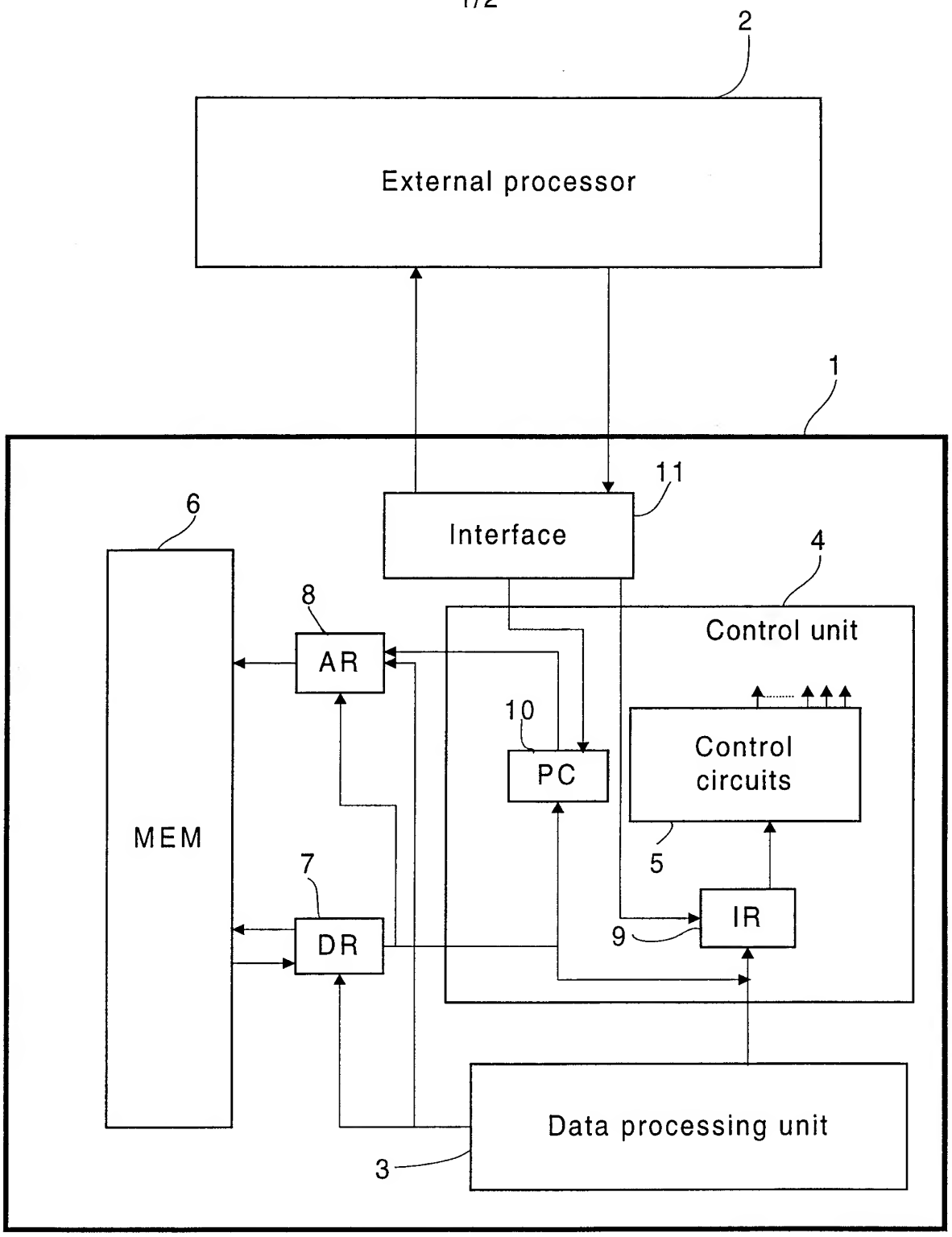
2
External processor
1
11
Interface
6
4
8
Control unit
AR
10
PC
Control
circuits
MEM
5
7
IR
9
DR
Data processing unit
3

FIG. 1

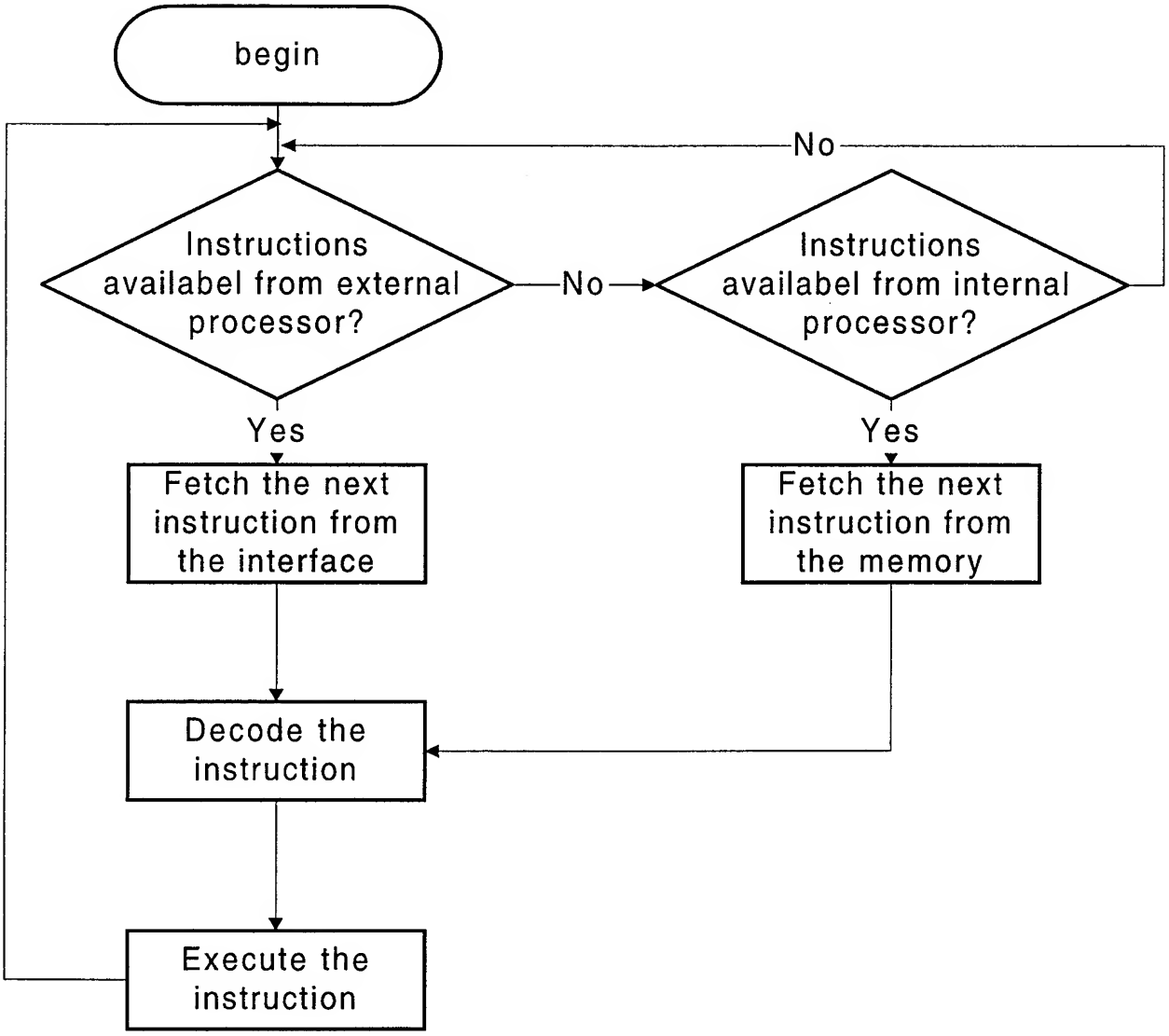
begin
No
Instructions availabel from external processor?
No
Instructions availabel from internal processor?
Yes
Yes
Fetch the next instruction from the interface
Fetch the next instruction from the memory
Decode the instruction
Execute the instruction

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 00/00040

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G06F 9/46, G06F 15/16
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0334526 A2 (DU PONT PIXEL SYSTEMS LIMITED), 27 Sept 1989 (27.09.89), column 5, line 21 - line 54, figure 1 --	1-7
D,A	US 5410544 A (J.A. KREIFELS ET AL.), 25 April 1995 (25.04.95), abstract -- --------	1-7

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0334526 A2	27/09/89	GB 2215873 A	27/09/89
		JP 2015378 A	19/01/90
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US 5410544 A	25/04/95	NONE	